

Day : Saturday
Date: 3/24/2007


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Inventor Name Search Result

Your Search was:

Last Name = PARTHASARATHY

First Name = VASUDEVAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>09391059</u>	Not Issued	77	09/07/1999	CODE MAPPING IN A TRELLIS DECODER	PARTHASARATHY, VASUDEVAN
<u>10694945</u>	Not Issued	71	10/29/2003	Apparatus and method for automatic polarity swap in a communications system	PARTHASARATHY, VASUDEVAN
<u>10767729</u>	Not Issued	30	01/30/2004	Method of monitoring the quality of a communications channel	PARTHASARATHY, VASUDEVAN
<u>10767748</u>	Not Issued	30	01/30/2004	System for monitoring the quality of a communications channel with mirror receivers	PARTHASARATHY, VASUDEVAN
<u>10813235</u>	Not Issued	30	03/31/2004	System and method of phase-locking a transmit clock signal phase with a receive clock signal phase	PARTHASARATHY, VASUDEVAN
<u>10813363</u>	Not Issued	30	03/31/2004	Transceiver device with a transmit clock signal phase that is phase-locked with a receiver clock signal phase	PARTHASARATHY, VASUDEVAN
<u>11124598</u>	Not Issued	30	05/05/2005	State based algorithm to minimize mean squared error	PARTHASARATHY, VASUDEVAN
<u>11292610</u>	Not Issued	30	12/02/2005	Receive equalizer with adaptive loops	PARTHASARATHY, VASUDEVAN
<u>60138232</u>	Not Issued	159	06/09/1999	CODE MAPPING IN A TRELLIS DECODER	PARTHASARATHY, VASUDEVAN
<u>60172920</u>	Not Issued	159	12/21/1999	TRUNCATED METRIC FOR NTSC INTERFERENCE REJECTION IN THE ATSC-HDTV TRELLIS DECODER	PARTHASARATHY, VASUDEVAN
<u>60540295</u>	Not Issued	159	01/30/2004	Transceiver device with a transmit clock signal phase that is phase-locked with a	PARTHASARATHY, VASUDEVAN

				receive clock signal phase	
<u>60737292</u>	Not Issued	159	11/15/2005	Receive equalizer with adaptive loops	PARTHASARATHY, VASUDEVAN
<u>60840123</u>	Not Issued	20	08/25/2006	Digital electronic dispersion compensation for multi-mode fiber	PARTHASARATHY, VASUDEVAN

Inventor Search Completed: No Records to Display.

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